VLSI Project Titles 2021-22

S.no	Title
1	VLSI Implementation of Error Detection and Correction Codes for Space Engineering
2	VLSI Design of a Squaring Architecture Based on Yavadunam Sutra of Vedic Mathematics
3	SMUL-FFT: A Streaming Multiplierless Fast Fourier Transform
4	Reliable CRC-Based Error Detection Constructions for Finite Field Multipliers With Applications in Cryptography
5	Pipeline Architecture for N=K*2L Bit Modular ALU: Case Study between Current Generation Computing and Vedic Computing
6	Parity Generator & Parity Checker Using Sub-threshold Adiabatic Logic
7	New Double Fault Tolerant Full Adder Design for Real-Time Applications
8	Matrix based Error Detection and Correction using Minimal Parity Bits for Memories
9	Low Power, High speed VLSI Circuits in 16nm Technology
10	Lossless EEG Compression Algorithm Based on Semi- Supervised Learning for VLSI Implementation
11	*Instant Access Memory Design based on an FPGA*
12	Improvement of Accuracy of Fixed-Width Booth Multipliers Using Data Scaling Technology
13	Design of digital circuit implementation using GDI and Cmos Technology
14	High-Parallelism Hash-Merge Architecture for Accelerating Join Operation
15	Fast Binary Counters and Compressors Generated by Sorting Network
16	*Low Complexity LDPC Error Correction Code for Modified Anderson PUF to Improve its Uniformity*
17	Power Reduction in Domino Logic using clock gating in CMOS Technology
18	Diagonal Hamming Based Multi-Bit Error Detection and Correction Technique for Memories
19	Design of I2C Master Core with AHB Protocol for High Performance Interface
20	Design Implementation and Analysis of Different SRAM Cell Topologies
21	Design of BIST(Built-In-Self-Test)Embedded Master-Slave communication using SPI Protocol

22	Design and Simulation of Optical Fiber Communication Link by Ethernet Protocol
23	Design and Implementation of Vehicle Data Transmission Protocol Based on PRESENT Algorithm
24	Design and Implementation of Low Power High Speed Robust 10T SRAM
25	Design and Implementation of an Efficient Dadda Multiplier Using Novel Compressors and Fast Adder
26	Design and Analysis of Serial Peripheral Interface for Automotive Controller
27	DECODING TECHNIQUE FOR LOW POWER DESIGN IN XILINX
28	Comparative Analysis of Different Clock Gating Techniques
29	Analysis and Comparison of Leakage Power Reduction Techniques for VLSI Design
30	Design and Implementation of Optimized Parameter Based Operational Amplifier for High Speed Analog Signal Processing

S.No	TITLE NAME
EGT – VLSI - 1	Design of Generic Floating Point Pipeline Based Arithmetic Operation for DSP Processor
EGT – VLSI - 2	Implementation of Efficient Modulo 2n Adders for Cryptographic Applications
EGT – VLSI – 3	Implementation of AES Using Composite Field Arithmetic for IoT Applications
EGT – VLSI – 4	Design of Area Optimized Arithmetic and Logical Unit for Microcontroller
EGT – VLSI – 5	Implementation of RNS and LNS based addition and subtraction Units for cryptography
EGT – VLSI – 6	Efficient Modular Adder Designs Based on Thermometer and One-Hot Coding
EGT – VLSI - 7	Area and Power Efficient 64-Bit Booth Multiplier
EGT – VLSI – 8	An Improved Hardware Architecture for modulo without Multiplication
EGT – VLSI - 9	Single Bit Fault Detecting ALU Design using Reversible Gates
EGT – VLSI - 10	The Method Of Low Power, High Performance And Area Efficient Address Decoder Design For SRAM
EGT – VLSI - 11	A Flexible Scan-in Power Control Method in Logic BIST and Its Evaluation with TEG Chips

EGT – VLSI - 12	Design Of High Performance Digital Divider
EGT – VLSI - 13	LFSR-based Bit-Serial GF(2m) Multipliers using Irreducible Trinomials
EGT – VLSI - 14	Efficient Modular Adder Designs Based on Thermometer and One-Hot Coding
EGT – VLSI - 15	Design and Implementation of Primitive Cells, Full Adder, Full Subtractor, and Multiplier using Modified Gate Diffusion Input Logic
EGT – VLSI - 16	Area Efficient Memory-Based Even-Multiple-Storage Multiplier for Higher Input
EGT – VLSI - 17	An Efficient Architecture for Signed Carry Save Multiplication
EGT – VLSI - 18	A Unified Architecture for AES/PRESENT Ciphers and its Usage in an SoC Environment
EGT – VLSI – 19	Input Test Data Volume Reduction Using Seed Complementation and Multiple LFSRs
EGT – VLSI - 20	Implementation of Square and Cube Architecture using Vedic Mathematics
EGT – VLSI - 21	Design of Modified Dual-CLCG Algorithm for Pseudo-Random Bit Generator
EGT – VLSI - 22	Design and Implementation of Encryption/ Decryption Architectures for BFV Homomorphic Encryption Scheme
EGT – VLSI - 23	A Novel Parametrized Fused Division and Square- Root POSIT Arithmetic Architecture
EGT – VLSI - 24	VLSI Architecture for High Performance Wallace Tree Encoder
EGT – VLSI - 25	Reduction of Power and Delay in Shift Register using MTCMOS Technique
EGT – VLSI - 26	High-Speed Area-Efficient VLSI Architecture of Three-Operand Binary Adder
EGT – VLSI - 27	Estimation of Power and Delay of CMOS Phase Detector and Phase-Frequency Detector Using Nano Dimensional MOS Transistor
EGT – VLSI - 28	Design and Analysis of Bulk and Junctionless MOSFET Based Circuits for Low Power Applications
EGT – VLSI - 29	Low Power Design of 4-bit Simultaneous Counter using Digital Switching Circuits for Low Range Counting Applications
EGT – VLSI - 30	Power Analysis of a Lossless Data Compression Technique